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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,962	02/10/2004	Nagamasa Mizushima	16869D-096500US	3583

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EXAMINER	
NGUYEN, THAN VINH	
ART UNIT	**PAPER NUMBER**
2187	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/776,962	MIZUSHIMA ET AL.	
	Examiner	Art Unit	
	Than Nguyen	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23,29 and 31-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-12,28 and 29* is/are allowed.

6)☒ Claim(s) *1,2,7,8,13-21 and 31* is/are rejected.

7)☒ Claim(s) *3-6,22,23 and 32-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is a response to the amendment, filed 1/11/07.

2. Claims 1-31 were pending. Claims 24-28, and 30 are canceled. Claims 32-34 are newly added. Claims 1-23,29,31-34 remain pending.

Response to Amendment

3. In view of the amendment to the claim 1, the previous rejection to claims 1-8 under 35 USC 112, second paragraph, is withdrawn.

4. In view of the amendment to the title, the previous objection to the title is withdrawn.

5. In view of the submitted certified copies of Japanese applications, the previous objection to the priority is withdrawn.

6. Applicant's arguments with respect to claims 1-23,29,31-34 have been considered but are moot in view of the new ground(s) of rejection. Applicant has amended the claims to include limitations not previously considered. The amended claims are addressed below.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 31 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 31 is dependent upon canceled claim 24. It has not been treated on its merits.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1,2,7,8, 13-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshino (US 6,003,113).

As to claim 1:

11. Hoshino teaches a portable card medium and method for managing memory space of the card medium. Hoshino teaches a memory device comprising: an interface which interfaces with an external device (connect interface, 11/1-4; Fig. 23); an IC chip (IC card 10) which comprises an EEPROM (memory 30; 11/1) for storing a plurality of application programs and a CPU for executing said application programs (CPU 20; 11/1); a nonvolatile memory which stores associated data associated with said one or more application programs (memory 30; 14/12-17)); and a controller (area controller mechanism 5) connected with said interface, said IC chip, and said memory; wherein said controller, in response to a predetermined command received from said external device by way of said interface, performs transfer of said associated data between said IC chip and said nonvolatile memory without passing said associated data to said host device during transfer of said associated data between said IC chip and said memory (CPU 20 accessing memory 30; 12/5-15). Hoshino does not specifically teach the IC chip, nonvolatile memory and controller are separate chips. It has been held that making elements separable

instead of integrated is obvious. In re Dulberg, 289 F.2d 522, 523, 129 USPQ 348, 349 (CCPA 1961). Thus, it would have been obvious to one of ordinary skills in the art to design the invention so that the IC chip, nonvolatile memory, and controller are separate chips to enable easy replacement of a failed item.

As to claim 2:

12. Hoshino teaches said nonvolatile memory is divided into a plurality of blocks (nonvolatile memory 30); and each of said plurality of blocks to be assigned to an application program to store said associated data associated with said assigned application program (applications assigned memory spaces; 14/12-17).

As to claim 7:

13. Hoshino teaches wherein said associated data is already stored in said nonvolatile memory when said memory device is first used (stored application and associated data in memory 30; 13/48-60).

As to claim 8:

14. Hoshino teaches said controller which performs transfer of associated data associated with an application program between said IC chip and said nonvolatile memory, in response to said predetermined command, by a transfer command associated with said application program sent from said memory to said IC chip (CPU access data from memory 30; 12/5-15).

As to claim 13:

15. Hoshino teaches an IC chip (IC card 10) which comprises an EEPROM (memory 30) for storing application programs and a CPU (CPU 20) for executing one or more application programs; a nonvolatile memory (memory 30; 14/12-17) divided into a plurality of blocks, each block to be assigned to an application program executed by said IC; and a controller controlling access to said nonvolatile memory and said IC chip (area control mechanism 5); wherein said controller, in response to a first command from an external device, assigns a usage privilege for a block in said nonvolatile memory to a particular application program to be executed by said IC chip (applications assigned memory spaces; 5/1-32; Fig. 5; 6/20-67); and, in response to a second command from the external device, changes from an unlocked state allowing execution of an operation in response to said first command to a locked state disallowing execution of said operation in response to said first command (access restriction to allow/block access; 14/52-15/4). Hoshino does not specifically teach the IC chip, nonvolatile memory and controller are separate chips. It has been held that making elements separable instead of integrated is obvious. In re Dulberg, 289 F.2d 522, 523, 129 USPQ 348, 349 (CCPA 1961). Thus, it would have been obvious to one of ordinary skills in the art to design the invention so that the IC chip, nonvolatile memory, and controller are separate chips to enable easy replacement of a failed item.

As to claim 14:

16. Hoshino teaches wherein said nonvolatile memory is controllable to operate in a locked mode to disable changing and adding and deleting an application ID in said memory associated with an application program stored in said IC chip when at least one application program is stored in said IC chip, and an unlocked mode to permit changing and adding and deleting an application ID in said memory (access restriction to allow/block access; 14/52-15/4).

As to claim 15:

17. Hoshino teaches wherein said nonvolatile memory management information used to manage associations between identifiers for said blocks and identifiers for application programs for which usage privilege has been assigned for said blocks; and said controller, when usage privilege for a block is assigned to an application program, adds an identifier for said application program to the management (application programs and associated privilege/security data; 13/48-67; 14/60-15/4).

As to claim 16:

18. Hoshino teaches said nonvolatile memory stores a flag for identifying whether execution of the operation in response to the first command is allowed for disallowed; and said controller changes said flag when changing from unlocked stat to lock state in response to the second command (access restriction to allow/block access; 14/52-15/4).

As to claim 17:

19. Hoshino teaches wherein said controller changes from said locked state to said unlocked state in response to a third command from said external device (set access authority; 14/52-55).

As to claim 18:

20. Hoshino teaches said nonvolatile memory stores a reference password; and said controller changes from said locked state to said unlocked state in response to said third command if a password received from said external device matches said reference password in said memory (determine if key match; 17/35-55).

As to claim 19:

21. Hoshino teaches wherein said controller disables usage privilege for a block assigned for an application program in response to a fourth command from said external device (set access authority; 14/52-55).

As to claim 20:

22. Hoshino teaches said memory stores management information used to manage associations between identifiers for said blocks and identifiers for application programs for which usage privilege has been assigned for said blocks (access control information; 13/57-67; 16/17-66); and said controller removes from said management information an identifier for said application program associated with an identifier for said block when disabling usage privilege for said block assigned for said application program (set access authority; 14/52-55).

As to claim 21:

23. Hoshino teaches wherein said memory includes a first area for storing data received from said external device and a second area comprising said blocks for which usage privilege is assigned for said application programs (storage areas for data and associated application data; Fig. 2).

Allowable Subject Matter

24. Claims 3-6, 22, 23, and 32-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

25. Claims 9-12, 28, 29 are allowed.

26. As to claim 3,15 the prior art does not teach wherein said nonvolatile memory includes a management area to store an association between an application ID used to identify each one of said application programs and an operation code used to transfer said associated data associated with said one application program between said nonvolatile memory and said IC chip through the controller.

27. Claims 4-6 and 32-34 are also allowable for incorporating the limitations of claim 3, and further limitations.

28. As to claim 9, the prior art of record does not teach the memory device as claimed. More specifically, the prior art does not teach said nonvolatile memory stores one or more command codes used to allow said controller to query said IC chip regarding an instruction to perform an operation, said instruction being issued by said IC chip to said controller, each command code being associated with an application ID for identifying an application program; wherein, in response to an application ID associated with an application program, said application ID in the IC chip being sent to the controller by said IC chip to said controller which executes said application program of said application ID, said controller identifies, out of said one or more command codes stored in said nonvolatile memory, a command code associated with said application ID from said IC chip, and sends said identified command code to said IC chip; and wherein, in response to an instruction to perform an operation issued by said IC chip to said controller based on said identified command code, said controller performs said operation.

29. Claims 10-12, 28, and 29 are also allowable for incorporating the limitations of claim 9, and further limitations.

30. As to claim 22, the prior art does not further teach the controller generates, for each application program, transfer command codes for identifying transfer commands for receiving data read from the second area of the nonvolatile memory from the IC chip and for sending data to be written to the second area of the IC chip.

31. Claim 23 is also allowable for incorporating the limitations of claim 22, and further limitations.

Conclusion

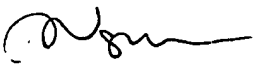
32. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 571-272-4198. The examiner can normally be reached on 8am-3pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Than Nguyen
Primary Examiner
Art Unit 2187